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Description

LIBRARY OF CELLS FOR USE IN DESIGNING SETS OF DOMINO LOGIC CIRCUITS IN A STANDARD CELL LIBRARY, OR THE LIKE, AND METHOD FOR USING SAME

Background of Invention

1. Field of Invention

[0001] This invention relates to improvements in circuit design methods, and more particularly to improvements in domino circuit design methods, and still more particularly to circuit libraries for use in performing such methods.

2. Relevant Background

[0002] Recently, circuit designers have been devoting increased interest to CMOS domino logic circuit designs, because of their reduced integrated circuit area, smaller parasitic capacitances, higher speed, and increased reliability.

[0003] Typically, domino logic circuits have an NMOS, or pull-down, logic portion, although PMOS pull-up logic circuits have been used in many applications. The logic portion serves to evaluate input logic signals to provide a conditional output signal to an output inverter.

[0004] Domino logic circuits also have a precharge transistor, typically a PMOS device when the logic circuit is made up with NMOS transistors, which is switched by the clock signal to connect the "dynamic node" of the circuit to a precharge voltage during a "precharge phase" of the clock cycle. The "dynamic node" may be for example, the output node of the logic circuit or the input node of the associated output inverter.

[0005] Thus, typically, the output inverter transistors are precharged during the precharge phase, while the clock signal is in a first state, low, for example, in an NMOS logic circuit implementation, or high in a PMOS logic circuit implementation. During the precharge phase, an "evaluate" transistor, whose gate is also connected to the clock signal, isolates the associated logic circuit from the precharge voltage.

[0006] When the particular logic conditions of the logic circuit are met during a subsequent "evaluate" phase when the clock

signal transitions from low to high in the NMOS logic circuit implementation, the output node of the logic circuit (the input of the inverter) is pulled down and the output of the inverter is pulled up. If the logic conditions of the logic circuit are not met, the output of the inverter remains low. Because the inverter is precharged when the clock signal transitions from low to high, the cell output can be developed very rapidly.

[0007] In the design of domino logic circuits, it will be appreciated that different applications require circuits of different speeds and driving abilities. However, usually a trade-off is involved, since in domino logic applications, usually faster circuits are larger in layout size, and consequently occupy more real estate of the substrate on which the circuit is constructed, and additionally consume more power. On the other hand, if the transistors of the logic circuit are made too large, they may unduly load the driver circuit. Consequently, in some applications, it may be that the driver circuit is large, while the associated logic circuitry is of relatively smaller devices, or vice versa. It can be seen that depending upon the particular application, large numbers of combinations of circuits may be required.

[0008] As a result, domino logic circuits had to be individually

designed to provide the necessary speed and drive power for a particular application. However, once the drive circuit has been designed, the associated logic circuit also had to be designed in accordance with the parameters of the drive circuit (or vice versa). As can be seen, this design process has been difficult and time consuming.

[0009] In efforts to standardize the design process, layout templates have been proposed into which the various domino circuit components can be placed in order to facilitate interconnection of a number of gates in a particular circuit. The arrangement of the various circuit parts in fixed layout regions provides a "standard cell", connectable to similar adjacent regions.

[0010] In one proposal, for example, a layout template is suggested for a domino logic circuit of the type having an n-FET logic tree. The n-FET logic tree is inserted into a first portion of the template. The output from the logic circuit is inverted in an output inverter, and latched by a p-FET device connected around the inverter. The p-FET portions of the inverter, a p-FET precharge transistor, and the p-FET latch transistor are inserted in predefined second template locations. The clock also includes an n-FET evaluate transistor, which is inserted into a third template

area.

[0011] However, in this and other previous proposals, the fixed layout template has not been concerned with the parametric characteristics of the ultimate cells, only the standardization of the layout template into which they are constructed to enable standardization of cell interconnections.

[0012] What is needed, therefore, is a method and circuit library for designing domino logic circuits to form a collection of domino logic cells that can be used for particular applications having varying drive power and speed requirements.

SUMMARY OF INVENTION

[0013] In light of the above, therefore, it is an object of the invention to provide a method and circuit library from which domino logic cell or gate sets can be constructed for particular applications having varying drive power, speed, or other parametric characteristic requirements.

[0014] An advantage of the invention is that sets of matchable circuits, namely, logic and drive circuits, can be selected to develop a library of circuits for a particular application. By "matchable", "match", "matching", or "matched" it is meant herein that the size, speed, capacitance, or other parametric characteristic of the circuits can be appropri-

ately interconnected for a desired result. The term is not intended to imply that the parametric characteristics of the logic and drive circuits are necessary the same, or even substantially the same.

[0015] Another advantage of the invention is that a library of domino circuits can be quickly developed, constructed, and completed.

[0016] Although layout templates may be used, they are not essential. The various sizes of the final circuits, which may constitute a library of "standard cells", may be fixed or variable, depending upon the particular uses to which the library that is developed is to be used. In some cases, however, the boundary locations of the circuits may be established to readily accommodate interconnection of various circuits that may result from the use of the circuit libraries defined by the invention.

[0017] According to a broad aspect of the invention, a set, family, or library of logic circuits is provided from which a desired logic function can be constructed. The transistors in the set have different sizes, speeds, capacitances, loading characteristics, or other parametric characteristics. Each circuit has an associated evaluate or "footer" transistor that is selected with the selection of the circuit. Addition-

ally, a set, family, or library of driver circuits is provided so that a driver can be selected to match the characteristics of the selected n-logic circuit, for example, in respect to sizes, speeds, capacitances, loading characteristics, or other parametric characteristics. A standard PMOS precharge transistor may be constructed, depending upon the characteristics of the circuit components selected from the libraries.

[0018] According to another broad aspect of the invention, a cell library is provided for use in designing integrated domino circuits. The cell library includes a first library portion including a plurality of FET logic circuits of first conductivity type to provide at least selectable transistor sizes. A second library portion includes a plurality of selectable prechargeable complementary FET driver circuits. Each of the driver circuits is configured to be connectable to an output of a selected one of the logic circuits, to provide selectable logic functions, transistor sizes, or other parametric characteristic.

[0019] According to yet another broad aspect of the invention, a cell library is provided for use in designing integrated circuits. The cell library includes a first library portion containing a plurality of NMOS logic circuits to provide se-

lectable logic functions and transistor sizes. A second library portion contains a plurality of selectable driver circuits, each configured to be connectable to an output of a selected one of the logic circuits. The driver circuits are selectable to match at least a size characteristic of the selected one of the logic circuits.

[0020] According to still another broad aspect of the invention, a cell library is provided. The cell library includes a plurality of selectable inverting NMOS logic circuits and a plurality of selectable inverter circuits. The inverter circuits are connectable to receive at least one output from a selected NMOS logic circuit.

[0021] According to yet another broad aspect of the invention, a method is presented for constructing an integrated circuit. The method includes selecting a logic circuit from a cell library containing a plurality of logic circuits and selecting a driver circuit from the cell library containing a plurality of driver circuits for connection to the selected logic circuit to match at least a size characteristic of the selected logic circuits.

Brief Description of Drawings

[0022] The invention is illustrated in the accompanying drawing, in which:

[0023] Figures 1a-d are circuit and layout diagrams of an example of an abbreviated library set of logic circuits that may be used in the construction of a library of domino circuits, in accordance with a preferred embodiment of the invention.

[0024] Figures 2a-d are circuit and layout diagrams of a library set of driver circuits that may be used in conjunction with selected logic circuits of Figures 1a-d in the construction of a library of domino circuits, in accordance with a preferred embodiment of the invention.

[0025] Figure 3 is a circuit and layout diagram of PMOS precharge transistor that may be used in conjunction with the logic and driver circuits of Figures 1a-d and 2a-c, in accordance with a preferred embodiment of the invention.

[0026] Figure 4 is a circuit and layout diagram of an example of a keeper circuit used in conjunction with the logic circuit of Figure 1c, in accordance with a preferred embodiment of the invention.

[0027] And Figure 5 is a circuit and layout diagram of an example circuit constructed using the library circuits of Figures 4, 2a, and 3, in accordance with a preferred embodiment of the invention.

[0028] In the various figures of the drawing, like reference nu-

merals are used to denote like or similar parts.

DETAILED DESCRIPTION

[0029] According to a preferred embodiment of the invention, a method and circuit library are provided. The library enables domino logic cell, gate, or circuit sets to be constructed for particular applications having varying drive power, speed, or other parametric characteristic requirements or having varying logic function requirements. Thus, with reference first to Figures 1a-d, an exemplar of a logic circuit set that may be included in a logic circuit collection from which domino logic circuits can be constructed is shown. From the logic circuit library of Figures 1a-d, a a set or library of circuits can be designed that have desired logic functions and parametric characteristics. In the library of Figures 1a-d, the various transistors have different sizes, speeds, capacitances, loading characteristics, or other parametric characteristics, and, as mentioned above, may be of appropriate polarity, i.e., NMOS or PMOS. In the examples herein, NMOS logic circuit functions are shown. The library example shown is abbreviated, showing only a few of the possible circuit configurations that can be presented for selection in the formation of a circuit library for a particular design appli-

cation.

[0030] More particularly, the circuits of Figures 1a-c show various selectable two-input NAND logic gates, the electrical schematic of which being shown on the left of the drawing and a corresponding representation of the layout of each circuit being shown on the right of the drawing. The layout representations show features that are only of approximate relative size, and show the implant, poly-1, contact, and selected metal-1 layers. Those skilled in the art will recognize the existence of various oxide or isolation layers between the various features shown.

[0031] Thus, as an example, the circuit 10 of Figure 1a of the abbreviated library has three transistors 12, 14, and 16 in series, which can be configured to receive respectively logic inputs A and B and the clock signal, CP, on their respective gates. In the layout diagram, the gate connections are labeled at respective contact features, and the corresponding metal-1 layers have been omitted for clarity. One end of the transistors 12, 14, and 16 is connected to a ground rail 18, and the output, Z, is derived at the other end on line or node 20.

[0032] The node 20 is selectively connectable to a driver circuit, described below in detail, and constitutes the dynamic

node that will be precharged in the operation of the domino circuit into which the circuit 10 may be incorporated. A typical metal-1 layer is shown connected to the contact 21 of transistor 12 to provide the output line, Z, 20. As can be seen, the transistors 12, 14, and 16 have a width-to-length (W/L) ratio respectively of 1.6u/0.13u, 2u/0.13u, and 2u/0.13u. This results in known transistor characteristics, notably the speed, capacitance, and drive capabilities of the devices, as well as other characteristics.

[0033] Similarly, the circuit 22 of Figure 1b of the abbreviated library has three transistors 24, 26, and 28 in series, which can be configured to receive respectively logic inputs A and B and the clock signal, CP. One end of the transistors 24, 26, and 28 is connected to the ground rail 18 at one end, and the output, Z, is derived at the other end on line or node 20. As can be seen, the transistors 24, 26, and 28 have a width-to-length (W/L) ratio respectively of 1.5u/0.13u, 1.5u/0.13u, and 1.5u/0.13u. This results in known transistor characteristics different from those of the circuit of Figure 1a.

[0034] Moreover, the circuit 30 of Figure 1c of the abbreviated library has three transistors 32, 34, and 36 in series, which can be configured to receive respectively logic inputs A

and B and the clock signal, CP. One end of the transistors 32, 34, and 36 is connected to the ground rail 18 at one end, and the output, Z, is derived at the other end on line or node 20. As can be seen, the transistors 32, 34, and 36 have a width-to-length (W/L) ratio respectively of 1u/0.13u, 1u/0.13u, and 1u/0.13u. This results in known transistor characteristics different from those of the circuits of Figures 1a and 1b.

[0035] The respective clock transistors 16, 28, and 36 will serve as the "evaluate" or "footer" transistor for the ultimate circuit to be constructed, in the selective matching combination of one of the circuits 10, 22, or 30 with a corresponding driver circuit described below in conjunction with Figures 2a-c.

[0036] Although the circuits of Figures 1a-c, which are exemplary only, have a two input NAND logic function, logic circuits of other logic functions, sizes, and parametric characteristics may also be included in the library, if desired. For example, as shown in Figure 1d, a three-input NAND gate embodiment 40 may be provided. Circuit embodiments having an OR functionality may also be provided, if desired. Furthermore, the library may contain circuits of particular custom physical architectures. As an

example, the transistor 12 the circuit 10 of Figure 1a is shown as having a length of 1.6 microns, to provide a tapered structure to the output to reduce its loading. The remaining transistors are shown having a length of 2 microns, illustrating the flexibility of the system.

[0037] Desirably, the set of circuits that are collected in the library contain most, if not all, of the parametric characteristics that will be needed in constructing the final library set from which the application circuits will be made. The library should also contain circuits having sufficient logic functionality to enable the particular logic functions to be used to be constructed. Typically, for example, a minimum library may contain a two-input NAND function and a two-input NOR function, since the logic circuits can be combined, as discussed below.

[0038] In addition to the library portion of logic circuits, according to a preferred embodiment of the invention, a library portion is provided having a set, family, or library of driver circuits. The driver circuit library is provided to enable a driver to be selected to match the characteristics of the selected logic circuit, for example, in respect to sizes, speeds, capacitances, loading characteristics, or other parametric characteristics. The driver circuits of Figures

2a-c are provided as an exemplar of a driver library that may be included. As with the logic circuit example of Figures 1a-d, various driver circuits are shown, the electrical schematic of which being shown on the left of the drawing and a corresponding representation of the layout of each circuit being shown on the right side of the drawing. The layout representations show features that are only of approximate relative size, and show the implant, poly-1, contact, and selected metal-1 layers. Those skilled in the art will recognize the existence of various oxide or isolation layers between the various features shown. Since a selected driver will be matched with a selected logic circuit, the driver circuits and logic circuits in each library should be designed with compatible manufacturing processes to enable them to be constructed as a part of the same integrated circuit.

[0039] Thus, with reference now additionally to Figure 2a, as an example, one circuit 45 that may be included in the library is an inverter having PMOS and NMOS transistors 46 and 48, connected between the supply rail, Vcc, 50, and the ground rail 18. The PMOS device 46 is formed in an n-well 52, and is of size, for example having a width-to-length (W/L) ratio of about 2u/0.13u. Only a single PMOS device

structure is formed in the layout (as compared to the multiple device structures of the embodiments of Figures 2b and 2c). Similarly, the NMOS device 48, which is of much smaller size, for example, has a width-to-length (W/L) ratio of about 0.7u/0.13u.

[0040] The input on input line 20 is connected to the corresponding output line 20 from a selected one of the logic circuits of Figures 1a-d, and the inverted output is derived on output line 54. In the layout diagram, the metal-1 layers have been omitted for clarity, except for the input line 20 and output line 54. As mentioned above, the node 20 will serve as the dynamic node that will be precharged in the operation of the domino circuit in which the circuit 55 may be incorporated.

[0041] With reference now additionally to Figure 2b, another example of an inverter circuit 55 that may be included in the library is shown. The inverter 55 has PMOS and NMOS transistors 56 and 58, connected between the supply rail, Vcc, 50, and the ground rail 18. The PMOS device 56 is formed in an n-well 52, and is of size, for example having a width-to-length (W/L) ratio of about 3.6u/0.13u. The width of the PMOS device is doubled using the two poly gate lines formed in the layout. Again, the NMOS device

58 is of much smaller size than the PMOS device, for example, having a width-to-length (W/L) ratio of about 0.7u/0.13u. This results in known transistor characteristics, notably the speed, capacitance, and drive capabilities of the devices, as well as other characteristics different from the circuit embodiment of Figure 2a.

[0042] The input on input line 20 is connected to the corresponding output line 20 from a selected one of the logic circuits of Figures 1a-d, and the inverted output is derived on output line 54. In the layout diagram, the metal-1 layers have been omitted for clarity, except for the input line 20 and output line 54. As mentioned above, the node 20 will serve as the dynamic node that will be precharged in the operation of the domino circuit in which the circuit 55 may be incorporated.

[0043] With reference now additionally to Figure 2c, still another example of an inverter circuit 60 that may be included in the library is shown. The inverter 60 has PMOS and NMOS transistors 62 and 64, connected between the supply rail, Vcc, 50, and the ground rail 18. The PMOS device 62 is formed in an n-well 52, and is of size, for example having a width-to-length (W/L) ratio of about 1.8u/0.26u. The NMOS device 64 is of much larger size than the NMOS de-

vice 58 of Figure 2b, for example, having a width-to-length (W/L) ratio of about 0.7u/0.26u. This results in known transistor characteristics, notably the speed, capacitance, and drive capabilities of the devices, as well as other characteristics different from the circuit embodiments of Figures 2a and 2b.

[0044] Again, the input on input line 20 is connected to the corresponding output line 20 from a selected one of the logic circuits of Figures 1a-d, and the inverted output is derived on output line 54. In the layout diagram, the metal-1 layers have been omitted for clarity, except for the input line 20 and output line 54. As mentioned above, the node 20 will serve as the dynamic node that will be precharged in the operation of the domino circuit in which the circuit 55 may be incorporated.

[0045] More particularly, in the design of typical domino circuits, the PMOS device of the driver is made very large and the NMOS device is made very small. However, Because the PMOS device is large, a large load can be driven, but it may load down the associated logic circuitry. So by having a family of sized devices available, a trade-off can be made to decrease the loading on the logic circuitry, and reduce the drive capacity of the PMOS device to optimize

the speed of the circuit. So, if a very large load is needed to be driven, the size of the PMOS device can be selected to accommodate that as well. In sum, different sized PMOS devices are available for different loading situations. On the other hand, a smaller driver slows down the n-logic less, so if a larger driver at the output is not necessary to drive the load, a smaller PMOS device may be chosen.

[0046] In order to precharge the dynamic node 20 of the circuit that is constructed using elements of the library exemplified by Figures 1a-d and 2a-c, a standard PMOS precharge transistor may be used. The parametric characteristics of the PMOS transistor may depend upon the characteristics of the circuit components selected from the libraries. Thus, with reference additionally now to Figure 3, a PMOS transistor 65 that can be used in conjunction with the circuit portions of Figures 1a-d and 2a-c is shown. The manufacturing processes by which the PMOS transistor is made should be compatible with the manufacturing processes of the circuits of the library portions with which it will be used to enable it to be constructed as a part of the same integrated circuit.

[0047] The PMOS precharge transistor 65 has the clock input, CP,

on its gate to conduct the supply voltage Vcc to the output line Z (the dynamic node), 20 when CP is low. In operation of the ultimate circuit, this will precharge the dynamic node 20 to enable domino operation. The PMOS transistor can be sized as needed, depending upon the particular circuit portions selected from the logic and driver circuit libraries. Various sized PMOS precharge transistors may be included as a part of the circuit libraries, if desired, or may be individually constructed for a particular circuit design as a standard transistor. Its size may be calculated, based upon known sizing parameters. Typically, in the construction of the standard cell libraries, a spot is left open during the initial design phases of the circuit, then a PMOS precharge transistor of predetermined size is inserted. Thus, if the drive PMOS transistor is small, the PMOS precharge transistor can also be made small, and vise versa.

[0048] If desired, keeper circuits may also be provided, for example, conveniently as a part of the logic circuit portion of the library. Usually a keeper circuit is desired in the design of a domino logic circuit; however, in some application, it may be desired to omit it. Consequently, the library may include some logic circuits having a keeper circuit, and

some circuits in which the keeper is omitted. The example circuit of Figure 4, to which reference is now additionally made shows a keeper circuit 70 associated with the logic circuit 30 of Figure 1c.

[0049] The keeper circuit 70 includes an inverter having a PMOS transistor 72 in series with an NMOS transistor 74 between the Vcc rail 50 and the ground rail 18. A weak PMOS transistor 76 is connected between the Vcc rail 50 and the dynamic node, Z, 20. The weak PMOS transistor 76 may be sized with a width-to-length (W/L) ratio of about 0.16u/0.13u, for example. As known, the weak PMOS transistor 76 serves to protect the dynamic node 20 from discharge that may be initiated by noise, current spikes, or the like.

[0050] In the layout of the keeper circuit, depending upon the size of the logic circuit with which it is associated, the location of the keeper circuit may need to be arranged to enable the insertion of the PMOS precharge transistor 65. As a result, various circuit arrangements may be provided in the library.

[0051] In performing the method according to a preferred embodiment of the invention, a circuit library can be constructed from the various circuit library portions of Fig-

ures 1a-d, 2a-c, 3, and 4. For example, a circuit 90, shown in Figure 5, to which reference is now additionally made, may be constructed from the circuits of Figures 4, 2a, and 3. The circuit 90 includes the logic portion 30, driver portion 45, precharge PMOS device 65, and keeper circuit 70, as described above. Through the selection of other combinations of the circuit library (only an exemplary portion of which being shown), other circuits can be designed having the logic function and parametric characteristics desired for a particular application. In the design of the final library, the various circuits may be manually constructed to form a library of cells. Then a synthesis tool may be used to construct the final circuit.

[0052] It should also be noted that in many circuit applications, the sizes of the various cells available in the library may be insufficient for the particular application needed. For example, if a logic function requiring an eight input AND gate is specified, the loading may be too much to maintain the desired speed or other circuit characteristic. Thus, it may be possible to provide two or more logic cells from the library, i.e., to split up the function among several logic cells. In that case, it may be necessary to provide driver circuits in the library that have multiple inputs, so

that the driver circuit itself may perform a NAND or NOR function to achieve the ultimate desired logic result. For example, two 4-input NOR gate logic circuits may be used to provide an input to a 2-input NAND driver circuit.

[0053] Although the invention has been described and illustrated with a certain degree of particularity, it should be understood that the description contained herein is made only by way of example, and that numerous changes in the arrangement and combination of parts may be made without departing from the spirit and scope of the invention, as hereinafter claimed.